

## (12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property  
Organization  
International Bureau



(43) International Publication Date  
15 April 2004 (15.04.2004)

PCT

(10) International Publication Number  
**WO 2004/032226 A1**

(51) International Patent Classification<sup>7</sup>: **H01L 21/762**

75, B-3001 Leuven (BE). **ROOYACKERS, Rita, V., T.**  
[BE/BE]; c/o Kapeldreef 75, B-3001 Leuven (BE).

(21) International Application Number:  
PCT/IB2003/004303

(74) Agent: **DUIJVESTIJN, Adrianus, J.**; Philips Intellectual  
Property & Standards, Prof. Holstlaan 6, NL-5656 AA  
Eindhoven (NL).

(22) International Filing Date:  
30 September 2003 (30.09.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:  
02079084.6 3 October 2002 (03.10.2002) EP

(71) Applicant (for all designated States except US): **KONIN-  
KLJKE PHILIPS ELECTRONICS N.V.** [NL/NL];  
Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU,  
AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU,  
CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE,  
GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR,  
KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK,  
MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT,  
RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR,  
TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(71) Applicant (for DE, FR, GB, JP only): **INTERUNIVER-  
SITAIR MICROELEKTRONICA CENTRUM VZW**  
[BE/BE]; Kapeldreef 75, B-3001 Leuven (BE).

(84) Designated States (*regional*): ARIPO patent (GH, GM,  
KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW),  
Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),  
European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE,  
ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO,  
SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM,  
GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

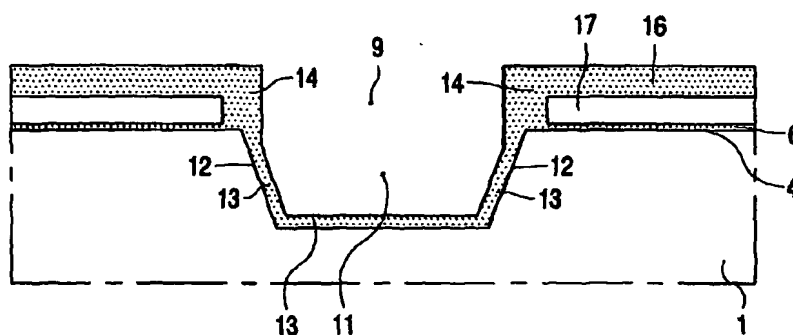
(72) Inventors; and

(75) Inventors/Applicants (for US only): **SCHMITZ, Ju-  
rriaan** [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA  
Eindhoven (NL). **RAVIT, Claire** [FR/BE]; c/o Kapeldreef

Published:  
— with international search report

[Continued on next page]

(54) Title: METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE WITH FIELD ISOLATION REGIONS CON-  
SISTING OF GROOVES FILLED WITH ISOLATING MATERIAL



(57) Abstract: A method of manufacturing a semiconductor device comprising a silicon body (1) having a surface (4) provided with field isolation regions (2) enclosing active regions (3). In this method, on the surface of the silicon body there is formed an auxiliary layer (5) of a material on which, during an oxidation treatment, a thicker layer of silicon oxide is formed than on the silicon of the silicon body. Here, an auxiliary layer comprising silicon and germanium is formed on the surface, said auxiliary layer preferably being a layer of SixGe1-x-yCy, where 0.70 < x < 0.95 and y < 0.05. Next, at the location of the field isolation regions to be formed, windows (9) are formed in the auxiliary layer and trenches (11) are formed in the silicon body. Next, on the walls (12) of the trenches, a silicon oxide layer (13) is provided and on the walls (10) of the windows a silicon oxide layer (14) is provided, both being formed by an oxidation treatment. The auxiliary layer is not oxidized throughout its thickness. After the oxidation treatment, a layer of insulating material (18) is deposited which fills the trenches and windows completely. Then, successively, a planarization treatment is carried out until the non-oxidized part of the auxiliary layer (17) is exposed, and the exposed part of the auxiliary layer is removed. Thus, field isolation regions (2) are formed having an edge (19) extending above the active regions (3).